DETAILED ACTION

1. This action is responsive to the following communication: Application filed on April 12, 2005, the Information Disclosure Statement filed on April 12, 2005, the Information Disclosure Statement filed on September 3, 2008, and the Foreign Priority filed on April 12, 2005.

2. Claims 1, 2, 4-15, and 20-22 are pending. Claims 3 and 16-19 are cancelled by Examiner's Amendment. Claims 1, 9, and 11-15 are currently amended by Examiner's Amendment. Claims 20-22 are new by Examiner's Amendment. Claims 1, 9, 13, 20, 21, and 22 are independent.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Johnny Ma (Reg. No. 59,976) on August 12, 2009.

Additionally, authorization to charge for the additional independent claim was given in a telephone interview with Johnny Ma (Reg. No. 59,976) on August 13, 2009.

In the Claims, replace **Claim 1** with the following:

--1. (Currently Amended) A memory device allowing charges accumulated in

capacitors of a plurality of memory cells connected to a plurality of activated word lines to be combined along one bit line, the device comprising:

activation means for activating the plurality of word lines simultaneously; and

signal output means for outputting a digital signal having a value that corresponds to a total amount of charges obtained along the one bit line by combining the charges accumulated in the capacitors of the plurality of memory cells connected to the plurality of word lines activated by the activation means,

wherein the plurality of memory cells connected to the one bit line includes cells having different maximum predetermined capacitance of their capacitors.--

In the Claims, replace **Claim 9** with the following:

--9. (Currently Amended) A memory device comprising:

a first frame memory portion including a plurality of memory cells connected to bit lines and word lines, respectively, and arranged in a matrix, to store an image signal of a first frame; and

a second frame memory portion including a plurality of memory cells connected to the bit lines and word lines, respectively, and arranged in the matrix, to store an image signal of a second frame,

wherein the first frame memory portion and the second frame memory portion are formed consecutively in a row direction, in which the bit lines extend;

wherein, in the first frame memory portion and the second frame memory portion, charges accumulated in capacitors of a plurality of memory cells connected to a plurality

of activated word lines can be combined along one bit line, the plurality of memory cells connected to the one bit line including cells having different maximum predetermined capacitance of their capacitors;

wherein, in each of the first frame memory portion and the second frame memory portion, the plurality of memory cells connected to each of the bit lines is divided into units, each including a predetermined number of memory cells that are connected to a predetermined number of word lines, to store one item of pixel data in each of these divided units;

wherein each unit of the first frame memory portion stores pixel data of the image signal of the first frame in straight binary format and each unit of the second frame memory portion stores pixel data of the image signal of the second frame in two's complement format, and

wherein the memory device further comprises:

activation means for simultaneously activating a plurality of word lines related to predetermined data in the first frame memory portion and a plurality of word lines related to predetermined data in the second frame memory portion;

bit line selection means for selecting any one of the plurality of bit lines; and

signal output means for outputting a digital signal having a value that corresponds to a total amount of charges obtained along the bit line selected by the bit line selection means.--

In the Claims, replace **Claim 13** with the following:

--13. (Currently Amended) A memory device comprising:

a memory portion including a plurality of memory cells connected to bit lines and word lines, respectively, and arranged in a matrix,

wherein, in the memory portion, charges accumulated in capacitors of a plurality of memory cells connected to a plurality of activated word lines can be combined along one bit line, the plurality of memory cells connected to the one bit line including cells having different maximum predetermined capacitance of their capacitors; and

wherein, in the memory portion, the plurality of memory cells connected to each of the bit lines is divided into units, each including a predetermined number of memory cells that are connected to a predetermined number of word lines, to store one item of data in each of these divided units,

the memory device further comprising:

activation means for simultaneously activating word lines related to plural items of data;

bit line selection means for selecting any one of the plurality of bit lines; and

signal output means for outputting a digital signal having a value that corresponds to a total amount of charges obtained along the bit line selected by the bit line selection means.--

In the Claims, add new **Claim 20** as follows:

--20. (New) A memory device allowing charges accumulated in capacitors of a

plurality of memory cells connected to a plurality of activated word lines to be combined along one bit line, the device comprising:

an activation unit configured to activate the plurality of word lines simultaneously; and

a signal output unit configured to output a digital signal having a value that corresponds to a total amount of charges obtained along the one bit line by combining the charges accumulated in the capacitors of the plurality of memory cells connected to the plurality of word lines activated by the activation unit,

wherein the plurality of memory cells connected to the one bit line includes cells having different maximum predetermined capacitance of their capacitors.--

In the Claims, add new **Claim 21** as follows:

--21. (New) A memory device comprising:

a first frame memory portion including a plurality of memory cells connected to bit lines and word lines, respectively, and arranged in a matrix, and configured to store an image signal of a first frame; and

a second frame memory portion including a plurality of memory cells connected to the bit lines and word lines, respectively, and arranged in the matrix, and configured to store an image signal of a second frame,

wherein the first frame memory portion and the second frame memory portion are formed consecutively in a row direction, in which the bit lines extend;

wherein, in the first frame memory portion and the second frame memory portion,

charges accumulated in capacitors of a plurality of memory cells connected to a plurality of activated word lines are configured to be combined along one bit line, the plurality of memory cells connected to the one bit line including cells having different maximum predetermined capacitance of their capacitors;

wherein, in each of the first frame memory portion and the second frame memory portion, the plurality of memory cells connected to each of the bit lines is divided into units, each including a predetermined number of memory cells that are connected to a predetermined number of word lines, and configured to store one item of pixel data in each of these divided units;

wherein each unit of the first frame memory portion is configured to store pixel data of the image signal of the first frame in straight binary format and each unit of the second frame memory portion is configured to store pixel data of the image signal of the second frame in two's complement format, and

wherein the memory device further comprises:

an activation unit configured to simultaneously activate a plurality of word lines related to predetermined data in the first frame memory portion and a plurality of word lines related to predetermined data in the second frame memory portion;

a bit line selection unit configured to select any one of the plurality of bit lines; and

a signal output unit configured to output a digital signal having a value that corresponds to a total amount of charges obtained along the bit line selected by

the bit line selection unit.--

In the Claims, add new **Claim 22** as follows:

--22. (New) A memory device comprising:

a memory portion including a plurality of memory cells connected to bit lines and word lines, respectively, and arranged in a matrix,

wherein, in the memory portion, charges accumulated in capacitors of a plurality of memory cells connected to a plurality of activated word lines are configured to be combined along one bit line, the plurality of memory cells connected to the one bit line including cells having different maximum predetermined capacitance of their capacitors; and

wherein, in the memory portion, the plurality of memory cells connected to each of the bit lines is divided into units, each including a predetermined number of memory cells that are connected to a predetermined number of word lines, and configured to store one item of data in each of these divided units,

the memory device further comprising:

an activation unit configured to simultaneously activate word lines related to plural items of data;

a bit line selection unit configured to select any one of the plurality of bit lines; and

a signal output unit configured to output a digital signal having a value that corresponds to a total amount of charges obtained along the bit line selected by

the bit line selection unit.--

In the Claims, **Claim 11**, line 3, change "position of pixel data" to --position of the pixel data--.

In the Claims, **Claim 12**, line 1, change "when one" to --when the one--.

In the Claims, **Claim 14**, line 1, change "when one" to --when the one--.

In the Claims, **Claim 15**, lines 8 and 9, change "between pixel data of a pixel positions" to --between pixel data of a pixel position--.

In the Claims, cancel **Claims 3 and 16-19.**

Information Disclosure Statement

4. Acknowledgment is made of Applicant's Information Disclosure Statement (IDS) Form PTO-1449 filed on April 12, 2005 and September 3, 2008. These IDS have been considered.

Priority

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Allowable Subject Matter

6. **Claims 1, 2, 4-15, and 20-22 are allowed.**

7. The following is an examiner's statement of reasons for allowance:

With respect to independent claim 1, there is no teaching, suggestion, or motivation for combination in the prior art to an activation means to activate the plurality of word lines simultaneously, a signal output means for outputting a digital signal having a value that corresponds to a total amount of charges obtained along the one bit line by combining the charges accumulated in the capacitors of the plurality of memory cells connected to the plurality of word lines activated by the activation means, wherein the plurality of memory cells connected to the one bit line includes cells having different maximum predetermined capacitance of their capacitors, in combination with the other limitations.

With respect to independent claim 9, there is no teaching, suggestion, or motivation for combination in the prior art to in the first frame memory portion and the second frame memory portion, charges accumulated in capacitors of a plurality of memory cells connected to a plurality of activated word lines can be combined along one bit line, the plurality of memory cells connected to the one bit line including cells having different maximum predetermined capacitance of their capacitors, wherein each unit of the first frame memory portion stores pixel data of the image signal of the first frame in straight binary format and each unit of the second frame memory portion stores

pixel data of the image signal of the second frame in two's complement format, and wherein the memory device further includes activation means for simultaneously activating a plurality of word lines related to predetermined data in the first frame memory portion and a plurality of word lines related to predetermined data in the second frame memory portion, and signal output means for outputting a digital signal having a value that corresponds to a total amount of charges obtained along the bit line, in combination with the other limitations.

With respect to independent claim 13, there is no teaching, suggestion, or motivation for combination in the prior art to in the memory portion, charges accumulated in capacitors of a plurality of memory cells connected to a plurality of activated word lines can be combined along one bit line, the plurality of memory cells connected to the one bit line including cells having different maximum predetermined capacitance of their capacitors, and wherein, in the memory portion, the plurality of memory cells connected to each of the bit lines is divided into units, each including a predetermined number of memory cells that are connected to a predetermined number of word lines, to store one item of data in each of these divided units, the memory device further includes activation means for simultaneously activating word lines related to plural items of data, and signal output means for outputting a digital signal having a value that corresponds to a total amount of charges obtained along the bit line selected by the bit line selection means, in combination with the other limitations.

With respect to independent claim 20, there is no teaching, suggestion, or motivation for combination in the prior art to an activation unit configured to activate the

plurality of word lines simultaneously, a signal output unit configured to output a digital signal having a value that corresponds to a total amount of charges obtained along the one bit line by combining the charges accumulated in the capacitors of the plurality of memory cells connected to the plurality of word lines activated by the activation unit, wherein the plurality of memory cells connected to the one bit line includes cells having different maximum predetermined capacitance of their capacitors, in combination with the other limitations.

With respect to independent claim 21, there is no teaching, suggestion, or motivation for combination in the prior art to in the first frame memory portion and the second frame memory portion, charges accumulated in capacitors of a plurality of memory cells connected to a plurality of activated word lines are configured to be combined along one bit line, the plurality of memory cells connected to the one bit line including cells having different maximum predetermined capacitance of their capacitors, wherein each unit of the first frame memory portion is configured to store pixel data of the image signal of the first frame in straight binary format and each unit of the second frame memory portion is configured to store pixel data of the image signal of the second frame in two's complement format, and wherein the memory device further includes an activation unit configured to simultaneously activate a plurality of word lines related to predetermined data in the first frame memory portion and a plurality of word lines related to predetermined data in the second frame memory portion, and a signal output unit configured to output a digital signal having a value that corresponds to a total amount of charges obtained along the bit line, in combination with the other limitations.

With respect to independent claim 22, there is no teaching, suggestion, or motivation for combination in the prior art to in the memory portion, charges accumulated in capacitors of a plurality of memory cells connected to a plurality of activated word lines are configured to be combined along one bit line, the plurality of memory cells connected to the one bit line including cells having different maximum predetermined capacitance of their capacitors, wherein, in the memory portion, the plurality of memory cells connected to each of the bit lines is divided into units, each including a predetermined number of memory cells that are connected to a predetermined number of word lines, and configured to store one item of data in each of these divided units, the memory device further includes an activation unit configured to simultaneously activate word lines related to plural items of data, and a signal output unit configured to output a digital signal having a value that corresponds to a total amount of charges obtained along the bit line, in combination with the other limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Ishii (U.S. Patent 5,134,582), Ogawa et al. (U.S. Patent

5,926,057), and Kondo et al. (U.S. Patent 7,573,939).

Ishii shows a memory to AND data bits along a column. However, Ishii does not show at least the plurality of memory cells connected to the one bit line includes cells having different maximum predetermined capacitance of their capacitors.

Ogawa et al. corresponds to 8-204567 (document number AM) cited on IDS filed April 12, 2005.

Kondo et al. show a related memory cell circuit and motion vector detection device. However, Kondo et al. do not show at least the plurality of memory cells connected to the one bit line includes cells having different maximum predetermined capacitance of their capacitors.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for

the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Tuan T. Nguyen/
Primary Examiner, Art Unit 2824
8/14/09

AGS